

700 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

The NCP137 is a 700 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP137 features low I_Q consumption. The WLCSP6 1.2 mm x 0.8 mm Chip Scale package is optimized for use in space constrained applications.

Features

- Input Voltage Range: V_{OUT} to 5.5 V
- Bias Voltage Range: 2.5 V to 5.5 V
- Adjustable and Fixed Voltage Version Available
- Output Voltage Range: 0.4 V to 1.8 V (Fixed) and 0.5 V to 3.0 V (Adjustable)
- $\pm 1\%$ Accuracy over Temperature, 0.5% V_{OUT} @ 25°C
- Ultra-Low Dropout: Typ. 40 mV at 700 mA
- Very Low Bias Input Current of Typ. 35 μ A
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μ A
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 4.7 μ F Ceramic Capacitor
- Available in WLCSP6 – 1.2 mm x 0.8 mm, 0.4 mm pitch Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders



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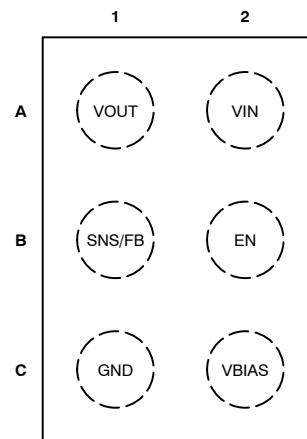
MARKING DIAGRAM

WLCSP6, 1.2x0.8
CASE 567MV

XXM▪

XX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

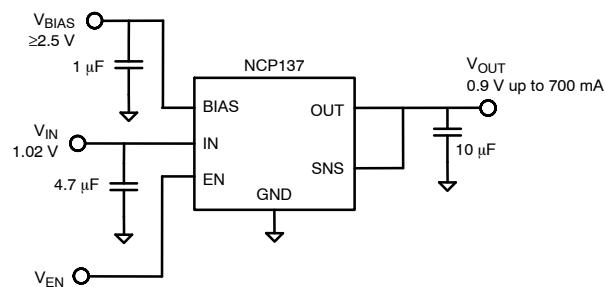
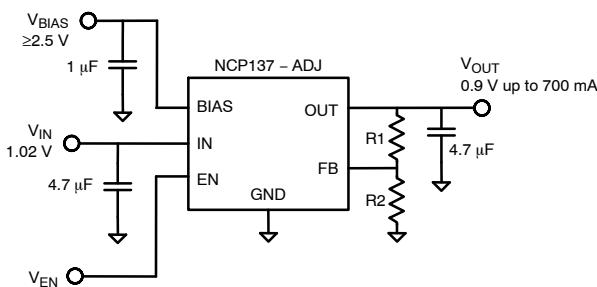
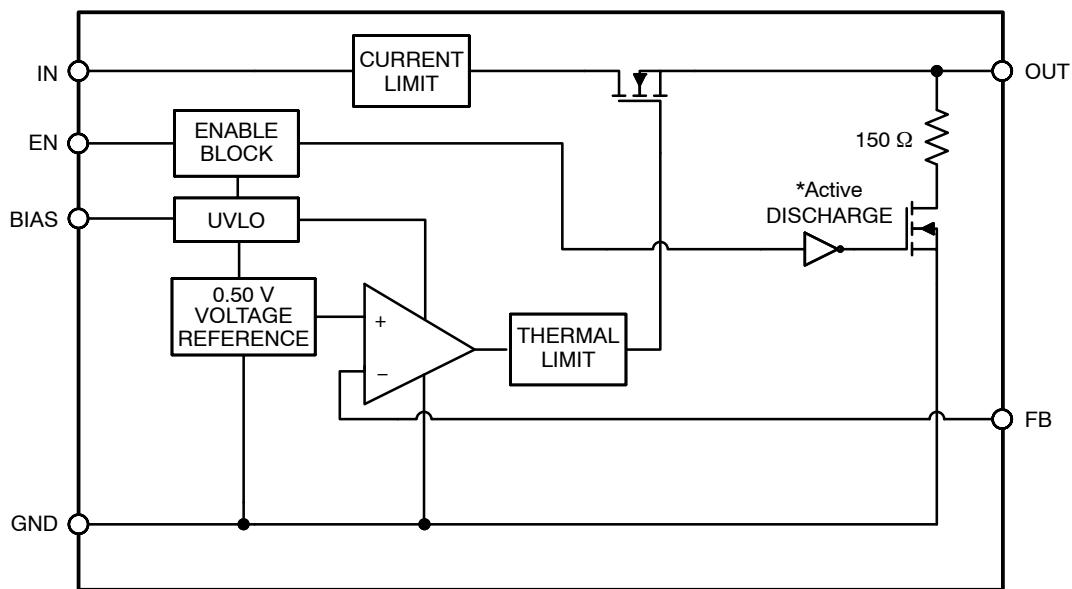


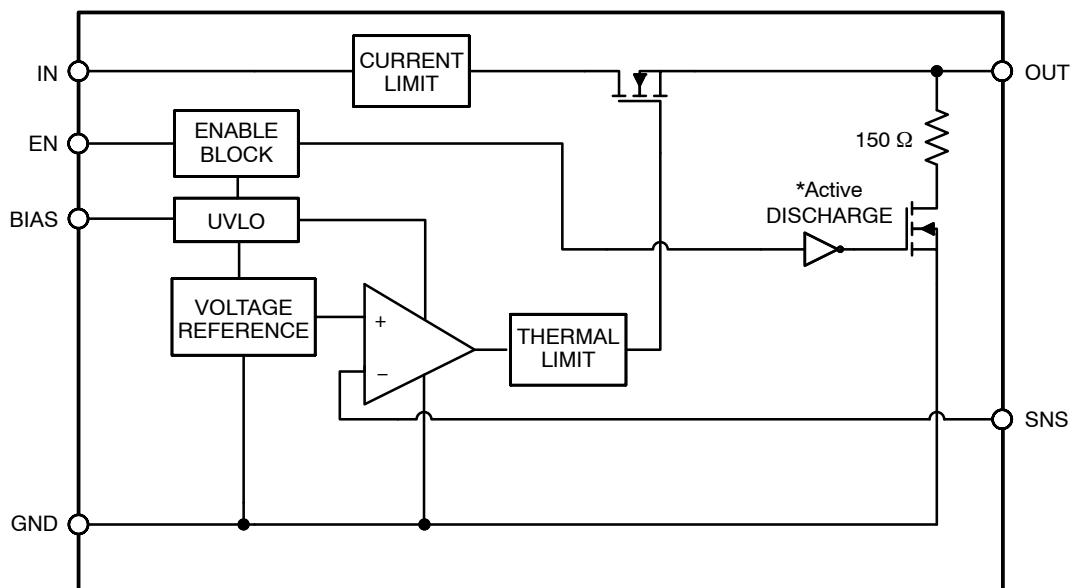
Figure 1. Typical Application Schematics

NCP137



*Active output discharge function is present only in NCP137A option devices.

Figure 2. Simplified Schematic Block Diagram – Adjustable Version



*Active output discharge function is present only in NCP137A option devices.

Figure 3. Simplified Schematic Block Diagram – Fixed Version

PIN FUNCTION DESCRIPTION

| Pin No. WLCSP6 | Pin Name | Description |
|--------------------------|----------|--|
| A1 | VOUT | Regulated Output Voltage pin |
| A2 | VIN | Input Voltage Supply pin |
| B1 (ADJ devices) | FB | Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node. |
| B1 (Fix Volt devices) | SNS | Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version. |
| B2 | EN | Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. |
| C1 | GND | Ground pin |
| C2 | VBIAS | Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit. |

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-------------------------------------|-------------------------------|------|
| Input Voltage (Note 1) | V_{IN} | -0.3 to 6 | V |
| Output Voltage | V_{OUT} | -0.3 to $(V_{IN}+0.3) \leq 6$ | V |
| Chip Enable, Bias, FB and SNS Input | $V_{EN}, V_{BIAS}, V_{FB}, V_{SNS}$ | -0.3 to 6 | V |
| Output Short Circuit Duration | t_{SC} | unlimited | s |
| Maximum Junction Temperature | T_J | 150 | °C |
| Storage Temperature | T_{STG} | -55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | ESD_{HBM} | 2000 | V |
| ESD Capability, Machine Model (Note 2) | ESD_{MM} | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
 ESD Human Body Model tested per EIA/JESD22-A114
 ESD Machine Model tested per EIA/JESD22-A115
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Thermal Characteristics, WLCSP6 1.2 mm x 0.8 mm Thermal Resistance, Junction-to-Air (Note 3) | $R_{\theta JA}$ | 69 | °C/W |

3. This junction-to-ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high-K (2s2p) 80 mm x 80 mm multilayer board with 1-ounce internal planes and 2-ounce copper on top and bottom. Top copper layer has a dedicated 1.6 sqmm copper area.

ELECTRICAL CHARACTERISTICS $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$; $V_{\text{BIAS}} = 2.7 \text{ V}$ or $(V_{\text{OUT}} + 1.6 \text{ V})$, whichever is greater, $V_{\text{IN}} = V_{\text{OUT}(\text{NOM})} + 0.3 \text{ V}$, $I_{\text{OUT}} = 1 \text{ mA}$, $V_{\text{EN}} = 1 \text{ V}$, $C_{\text{IN}} = 4.7 \mu\text{F}$, $C_{\text{OUT}} = 10 \mu\text{F}$, $C_{\text{BIAS}} = 1 \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^\circ\text{C}$. Min/Max values are for $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ unless otherwise noted. (Notes 4, 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|--|--|---------------------------------|------------------------------------|---|------|----------------------------|
| Operating Input Voltage Range | | V_{IN} | $V_{\text{OUT}} + V_{\text{DO}}$ | | 5.5 | V |
| Operating Bias Voltage Range | | V_{BIAS} | $(V_{\text{OUT}} + 1.50) \geq 2.5$ | | 5.5 | V |
| Undervoltage Lock-out | V_{BIAS} Rising Hysteresis | UVLO | | 1.6 0.2 | | V |
| Reference Voltage (Adj devices) | $T_J = +25^\circ\text{C}$ | V_{REF} | | 0.500 | | V |
| Output Voltage Accuracy | | V_{OUT} | | ± 0.5 | | % |
| Output Voltage Accuracy | $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$, $V_{\text{OUT}(\text{NOM})} + 0.3 \text{ V} \leq V_{\text{IN}} \leq V_{\text{OUT}(\text{NOM})} + 1.0 \text{ V}$, 2.7 V or $(V_{\text{OUT}(\text{NOM})} + 1.6 \text{ V})$, whichever is greater $< V_{\text{BIAS}} < 5.5 \text{ V}$, $1 \text{ mA} < I_{\text{OUT}} < 700 \text{ mA}$ | V_{OUT} | -1.0 | | +1.0 | % |
| V_{IN} Line Regulation | $V_{\text{OUT}(\text{NOM})} + 0.3 \text{ V} \leq V_{\text{IN}} \leq 5.0 \text{ V}$ | Line _{Reg} | | 0.01 | | %/V |
| V_{BIAS} Line Regulation | 2.7 V or $(V_{\text{OUT}(\text{NOM})} + 1.6 \text{ V})$, whichever is greater $< V_{\text{BIAS}} < 5.5 \text{ V}$ | Line _{Reg} | | 0.01 | | %/V |
| Load Regulation | $I_{\text{OUT}} = 1 \text{ mA}$ to 700 mA | Load _{Reg} | | 1.5 | | mV |
| V_{IN} Dropout Voltage | $I_{\text{OUT}} = 700 \text{ mA}$ (Notes 6, 7) | V_{DO} | | 40 | 60 | mV |
| V_{BIAS} Dropout Voltage | $I_{\text{OUT}} = 700 \text{ mA}$, $V_{\text{IN}} = V_{\text{BIAS}}$ (Notes 6, 8, 9) | V_{DO} | | 1.1 | 1.5 | V |
| Output Current Limit | $V_{\text{OUT}} = 90\% V_{\text{OUT}(\text{NOM})}$ | I_{CL} | 800 | 1200 | 1500 | mA |
| FB/SNS Pin Operating Current | | $I_{\text{FB}}, I_{\text{SNS}}$ | | 0.1 | 0.5 | μA |
| Bias Pin Quiescent Current | $V_{\text{BIAS}} = 2.7 \text{ V}$, $I_{\text{OUT}} = 0 \text{ mA}$ | I_{BIASQ} | | 35 | 50 | μA |
| Bias Pin Disable Current | $V_{\text{EN}} \leq 0.4 \text{ V}$ | $I_{\text{BIAS(DIS)}}$ | | 0.5 | 1 | μA |
| Vinput Pin Disable Current | $V_{\text{EN}} \leq 0.4 \text{ V}$ | $I_{\text{VIN(DIS)}}$ | | 0.5 | 1 | μA |
| EN Pin Threshold Voltage | EN Input Voltage "H" | $V_{\text{EN(H)}}$ | 0.9 | | | V |
| | EN Input Voltage "L" | $V_{\text{EN(L)}}$ | | | 0.4 | |
| EN Pull Down Current | $V_{\text{EN}} = 5.5 \text{ V}$ | I_{EN} | | 0.3 | 1 | μA |
| Turn-On Time | From assertion of V_{EN} to $V_{\text{OUT}} = 98\% V_{\text{OUT}(\text{NOM})}$. $V_{\text{OUT}(\text{NOM})} = 1.0 \text{ V}$, $C_{\text{OUT}} = 4.7 \mu\text{F}$ | t_{ON} | | 150 | | μs |
| Power Supply Rejection Ratio (Adj devices) | V_{IN} to V_{OUT} , $f = 1 \text{ kHz}$, $I_{\text{OUT}} = 10 \text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$, $V_{\text{OUT}(\text{NOM})} = 1.0 \text{ V}$, $C_{\text{OUT}} = 4.7 \mu\text{F}$ | PSRR(V_{IN}) | | 75 | | dB |
| | V_{BIAS} to V_{OUT} , $f = 1 \text{ kHz}$, $I_{\text{OUT}} = 10 \text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$, $V_{\text{OUT}(\text{NOM})} = 1.0 \text{ V}$, $V_{\text{BIAS}} = 3.0 \text{ V}$, $C_{\text{OUT}} = 4.7 \mu\text{F}$ | PSRR(V_{BIAS}) | | 85 | | dB |
| Output Noise Voltage (Adj devices) | $V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$, $f = 10 \text{ Hz}$ to 100 kHz , $V_{\text{OUT}(\text{NOM})} = 1.0 \text{ V}$, $C_{\text{OUT}} = 4.7 \mu\text{F}$ | V_N | | $35 \times V_{\text{OUT}}/V_{\text{REF}}$ | | μV_{RMS} |
| Thermal Shutdown Threshold | Temperature increasing | | | 160 | | $^\circ\text{C}$ |
| | Temperature decreasing | | | 140 | | |

- Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^\circ\text{C}$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
- Adjustable devices tested at $V_{\text{OUT}} = V_{\text{REF}}$ unless otherwise noted; external resistor tolerance is not taken into account.
- Dropout voltage is characterized when V_{OUT} falls 3% below $V_{\text{OUT}(\text{NOM})}$.
- For adjustable devices, V_{IN} dropout voltage tested at $V_{\text{OUT}(\text{NOM})} = 2 \times V_{\text{REF}}$.
- For adjustable devices, V_{BIAS} dropout voltage tested at $V_{\text{OUT}(\text{NOM})} = 3 \times V_{\text{REF}}$ due to a minimum Bias operating voltage of 2.5 V.
- For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$; $V_{\text{BIAS}} = 2.7 \text{ V}$ or $(V_{\text{OUT}} + 1.6 \text{ V})$, whichever is greater, $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3 \text{ V}$, $I_{\text{OUT}} = 1 \text{ mA}$, $V_{\text{EN}} = 1 \text{ V}$, $C_{\text{IN}} = 4.7 \mu\text{F}$, $C_{\text{OUT}} = 10 \mu\text{F}$, $C_{\text{BIAS}} = 1 \mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$. Min/Max values are for $-40^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$ unless otherwise noted. (Notes 4, 5)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|--|---|--------------------------------|-----|-----|-----|------------------|
| Output Discharge Pull-Down | $V_{\text{EN}} \leq 0.4 \text{ V}$, $V_{\text{OUT}} = 0.5 \text{ V}$, NCP137A options only | R_{DISCH} | | 150 | | Ω |
| Power Supply Rejection Ratio (Fixed Voltage devices) | V_{IN} to V_{OUT} , $f = 1 \text{ kHz}$, $I_{\text{OUT}} = 10 \text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$, $V_{\text{OUT(NOM)}} = 1.05 \text{ V}$, $C_{\text{OUT}} = 10 \mu\text{F}$ | $\text{PSRR}(V_{\text{IN}})$ | | 75 | | dB |
| | V_{BIAS} to V_{OUT} , $f = 1 \text{ kHz}$, $I_{\text{OUT}} = 10 \text{ mA}$, $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5 \text{ V}$, $V_{\text{OUT(NOM)}} = 1.05 \text{ V}$, $V_{\text{BIAS}} = 3.0 \text{ V}$, $C_{\text{OUT}} = 10 \mu\text{F}$ | $\text{PSRR}(V_{\text{BIAS}})$ | | 85 | | dB |
| Output Noise Voltage (Fixed Voltage devices) | $V_{\text{IN}} = V_{\text{OUT}} + 0.5 \text{ V}$, $f = 10 \text{ Hz}$ to 100 kHz , $V_{\text{OUT(NOM)}} = 1.05 \text{ V}$, $C_{\text{OUT}} = 10 \mu\text{F}$ | V_N | | 40 | | μVRMS |

- Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^{\circ}\text{C}$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
- Adjustable devices tested at $V_{\text{OUT}} = V_{\text{REF}}$ unless otherwise noted; external resistor tolerance is not taken into account.
- Dropout voltage is characterized when V_{OUT} falls 3% below $V_{\text{OUT(NOM)}}$.
- For adjustable devices, V_{IN} dropout voltage tested at $V_{\text{OUT(NOM)}} = 2 \times V_{\text{REF}}$.
- For adjustable devices, V_{BIAS} dropout voltage tested at $V_{\text{OUT(NOM)}} = 3 \times V_{\text{REF}}$ due to a minimum Bias operating voltage of 2.5 V.
- For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

APPLICATIONS INFORMATION

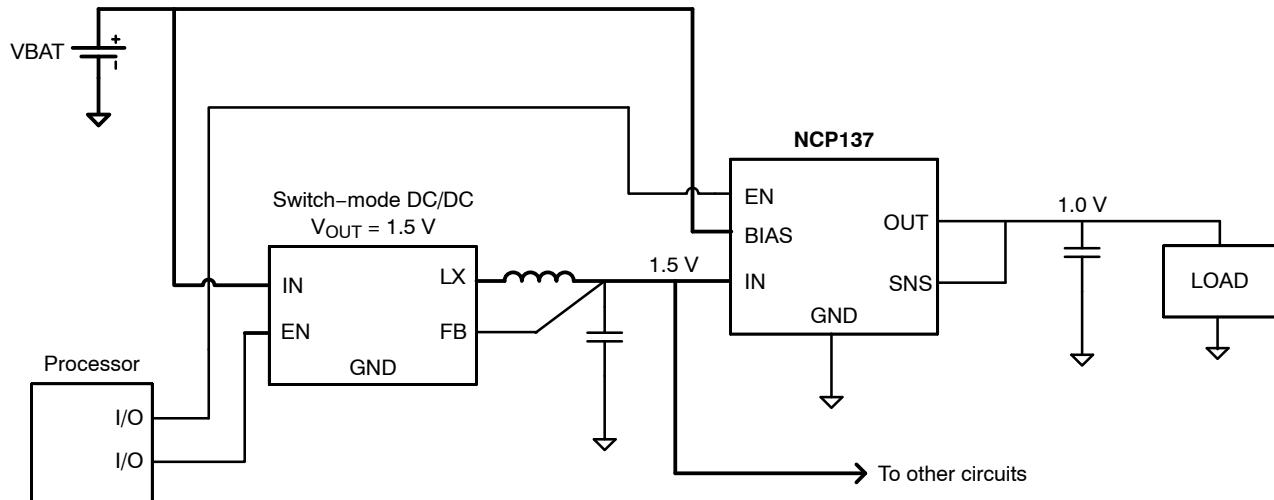


Figure 4. Typical Application: Low-Voltage DC/DC Post-Regulator with ON/OFF Functionality

The NCP137 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to V_{OUT} operating voltage difference can be very low compared with standard PMOS regulators in very low V_{IN} applications.

The NCP137 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis. NCP137 Voltage linear regulator Fixed and Adjustable version is available.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from 0.5 V to 3.0 V using two external resistors.

Typical application schematics is shown in Figure 5.

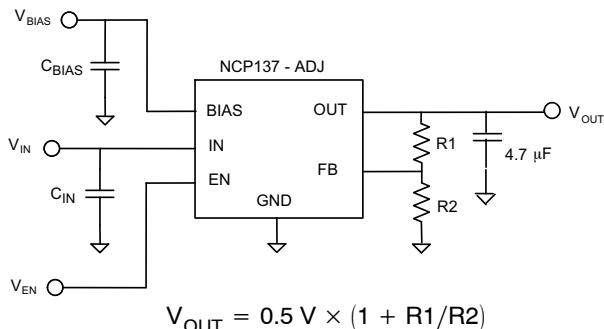


Figure 5. Typical Application Schematics

It is recommended to keep the total serial resistance of resistors ($R1 + R2$) no greater than 100 kΩ.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} - V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough; specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} - V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The Adjustable device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 4.7 μF to 22 μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range. For ADJ applications with nominal output voltage less than 0.6 V and for all the fixed voltage devices applications the output capacitor effective capacitance 10 μF to 22 μF is recommended.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended $C_{IN} = 1 \mu F$ and $C_{BIAS} = 0.1 \mu F$ or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to the NCP137 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +105°C maximum.

ORDERING INFORMATION

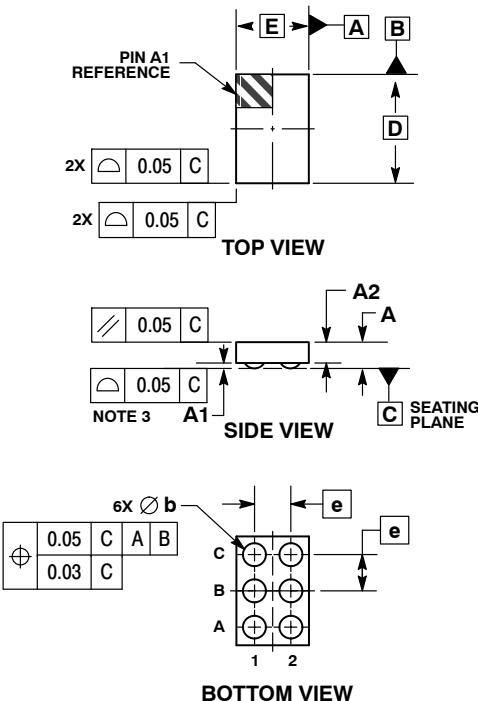
| Device | Nominal Output Voltage | Marking | Option | Package | Shipping [†] |
|-------------------|------------------------|---------|--|---------------------|-----------------------|
| NCP137AFCTADJT2G | ADJ | A7 | Output Active Discharge | WLCSP6 (Pb-Free) | 5000 / Tape & Reel |
| NCP137AFCTCADJT2G | ADJ | A7 | Output Active Discharge, Back Side Coating | | |
| NCP137BFCTADJT2G | ADJ | D7 | Non-Active Discharge | | |
| NCP137AFCT045T2G | 0.45 V | AT | Output Active Discharge | | |
| NCP137AFCT105T2G | 1.05 V | AA | Output Active Discharge | | |
| NCP137AFCT110T2G | 1.10 V | AH | Output Active Discharge | | |
| NCP137AFCTC110T2G | 1.10 V | AH | Output Active Discharge, Back Side Coating | | |
| NCP137AFCT120T2G | 1.20 V | AD | Output Active Discharge | | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON Semiconductor sales representative

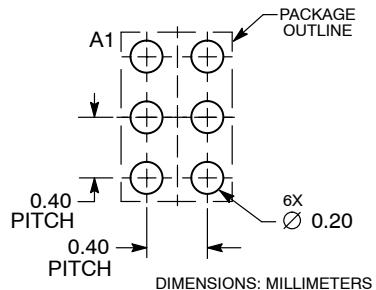
PACKAGE DIMENSIONS

WL CSP6, 1.20x0.80
CASE 567MV
ISSUE B



NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 0.33 |
| A1 | 0.04 | 0.08 |
| A2 | 0.23 REF | |
| b | 0.24 | 0.30 |
| D | 1.20 BSC | |
| E | 0.80 BSC | |
| e | 0.40 BSC | |

RECOMMENDED
SOLDERING FOOTPRINT*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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